A Novel MMIC PHEMT Low Noise Amplifier for GPS Applications

H. Morkner, M. Frank, R. Kishimura

Avantek (A subsidiary of Hewlett-Packard)
3175 Bowers Av. ,Santa Clara, CA 95054

ABSTRACT

A monolithic two stage PHEMT low-noise amplifier has been developed for the GPS and Spread Spectrum Bands (covering 0.5 to 3.0 GHz). This amplifier uses Avantek's advanced pseudomorphic HEMT (PHEMT) devices with sub 0.2-um gate-length and 0.25 dB noise figures in this band. The amplifier is unique in its usage of a source follower second stage, resistive feedback, and on-chip matching. Gain of 15 dB and noise figure of 1.7 dB have been measured. Designed to fit into a plastic 86 or SOT-143 surface mount package, the die is small (0.375 mm sq.), draws low current (<15mA), utilizes low voltage (3.3V), and has no bias choke requirement. This MMIC LNA has the best noise figure-to-gain-to-match-to-DC power performance of any product known, advertised or published.

INTRODUCTION

While HEMT and PHEMT demonstrate superior gain and noise figure performance over conventional MESFETs and Bipolars [1], not much work has been done with PHEMT in the GPS and Spread Spectrum bands. Typically, PHEMT FETs exhibit too much instability to be used in discrete form in the 0.5 GHz to 3.0 GHz band. There is an increasing need, however, for low noise, low DC power, low cost, front end amplifiers for GPS and Spread Spectrum applications. Available MMICs, such as the Triquint TQ9121 or Texas Instruments 8061, consume over 100 mW of power to deliver noise figures in excess of 2.0dB. This paper describes a low noise, low cost MMIC that utilizes a unique bias and matching scheme. The result is an untuned noise figure below 1.7dB, gain greater than 15dB, and a DC power requirement less than 50 mW.

DEVICE AND FABRICATION

The devices used in this monolithic design were pseudomorphic high electron mobility transistor (PHEMT) structures built using molecular beam epotaxy (MBE) material growth techniques. A cross section of the PHEMT structure used on this MMIC is shown in Figure 1. The gates were defined using electron-beam lithography. The results were lengths from 0.12 to 0.17 microns. A mushroom shaped gate was formed in order to reduce gate parasitic resistance by increasing the gate's cross sectional area.[2]

The design's primary amplification device consists of an interdigitated 300 um structure made up of a single gate feed which branches into four parallel gate fingers 75 um long. The typical DC characteristics of these devices are an Idss of 105 mA (0.35A/mm) with a pinch off voltage of -0.9V and a transconductance of 100 mS (330 S/mm). From measured on wafer I-V curves and s-parameters, a small signal equivalent model was constructed as shown in Figure 2. Table 1 shows typical

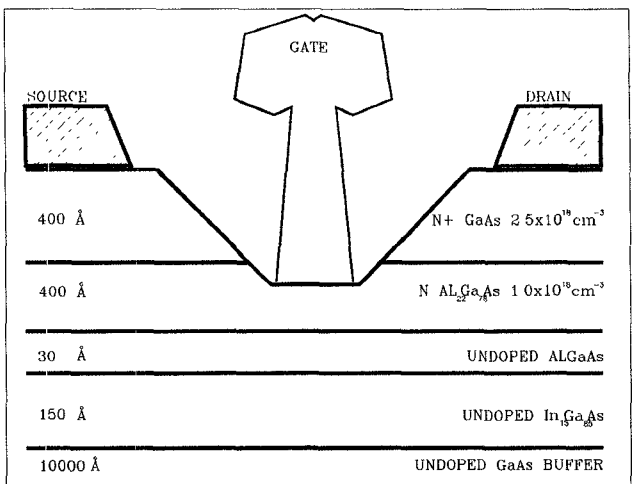

Figure 1. Physical vertical structure of a PHEMT

92CH3162-5/92/0000-0013$01.00 © 1992 IEEE

values used for parameter elements. In addition, a library of noise and s-parameters were measured (5% to 40% of Idss) on the Cascade Noise Parameter Test system [3].

The design uses a patented GaAs FET interdigitated 54 um current source as a saturated resistor for bias and RF signal blockage[4, 5]. The current source consists of a single finger PHEMT with the gate and source connected together. The design characteristics are modeled using the Table 1 parameters. The devices typically have an Idss of 15 mA and provide an -0.7V offset. Final noise and s-parameters for the device are determined through on wafer probing.

In addition to these active devices, the monolithic design makes use of wrap around for source grounding, air-bridges for interconnect, and MIM capacitors using silicon nitride for RF grounding and DC blocking. Resistors in the feedback are built using the natural 300 ohms/square bulk active material resistance.

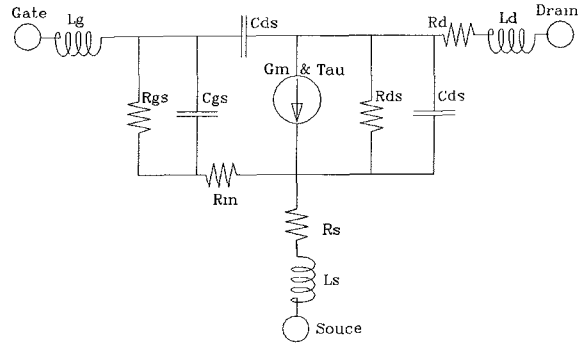

Figure 2. Equivalent circuit model of a PHEMT device.

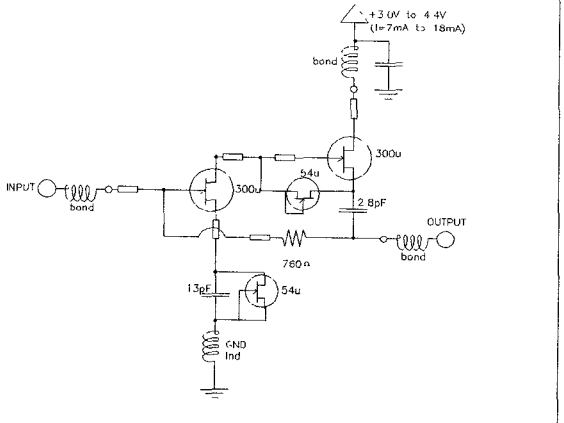

Figure 3. Schematic diagram for the monolithic 0.5 to 3.0 GHz PHEMT low noise amp.

MONOLITHIC LOW NOISE AMPLIFIER DESIGN

The MMIC amplifier was primarily designed using Libra[5], a software microwave simulation program from EEsof. The model was first used to determine circuit topology, first and second stage FET size, the current source size, and capacitor sizes. DC bias and coarse RF characteristics can be determined using the models and Libra options. The next step was to insert measured on wafer noise and s-parameter files to replace active device models in the simulation. This required measured data on the active devices over the voltage, current, and frequencies of interest. The feedback resistor and capacitor were selected for the optimum balance of noise figure and match. A minimum source RF bypass capacitor was selected for low frequency cut off. Various package and transmission line characteristics were included into the simulation to ensure stability and functionality in GPS and Spread Spectrum applications.

The result is a compact, process tolerant, low noise amplifier. Figure 3 has a schematic layout and Figure 4 a photograph of the amplifier.The input pad feeds directly into the gate of the first stage 300 um FET. No series or shunt inductance is added. The drain of the first stage FET feeds into the gate of the second stage 300 um FET. The drain of the second stage leads directly to the DC bias pad, while the source leads directly to the DC blocking capacitor on the output. A short 760 ohm resistive path directly connects the input to output to provide feedback. The feedback improves stability and input match while only slightly degrading the noise figure

EQUIVALENT CIRCUIT COMPONENT	UNIT	NAME	VALUE
Magnitude of Transconductance	mS	Gm	114 2
Gate-to-Source capacitance	pF	Cgs	0 211
Gate-to-Drain capacitance	pF	Cgd	0 060
Drain-to-Source capacitance	pF	Cds	0 090
Time delay associated with gm	pS	Tau	0 70
Gate resistance	Ohm	Rgs	13 2K
Channel resistance	Ohm	Rin	4 13
Source resistance	Ohm	Rs	1 43
Drain-to Source resistance	Ohm	Rds	73 2
Drain resistance	Ohm	Rd	4 82
Gate inductance	nH	Lg	0 039
Source inductance	nH	Ls	0 005
Drain inductance	nH	Ld	0 059
Calculated Ft = 60 GHz			

Table 1. Extracted equivalent model parameters.

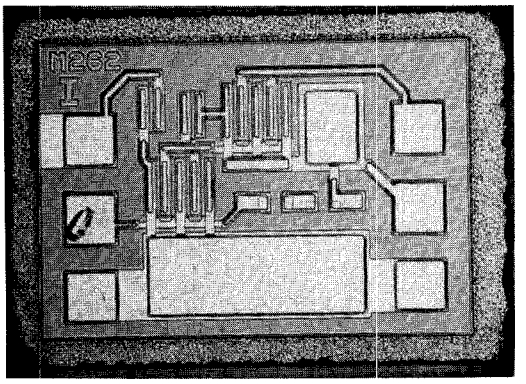

Figure 4. Monolithic PHEMT low noise amplifier. Chip size 0.725mm X 0.515mm.

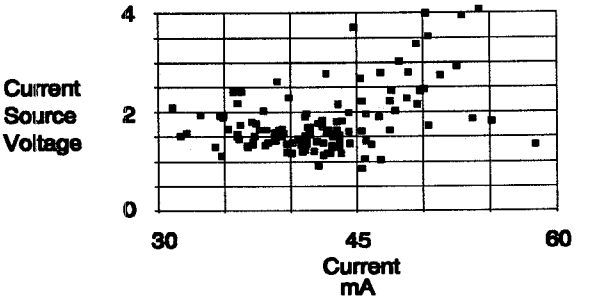

Figure 6. A PHEMT 100u current source saturated current vs. voltage distribution.

and output match. Current is shared from the second stage source to the first stage drain through a 54 um current source. A similar sized current source is connected in parallel with the large 13 pF first stage source capacitor to supply source bias.

The unique topology of sharing current through second stage FET - to - current source - to - first stage FET - to - current source causes equal distribution of voltage over a wide range of Idss and pinch off voltage. The bias scheme allows the circuit to present the same voltage to the active device, even when the device itself ranges across a large variation in dc parameters. Figure 5 is a plot of Idss vs. pinch off Voltage for a typical run of PHEMTs. Traditional resistor based biasing would lead to a large variation of bias. Figure 6 shows the bias across a current source, from this same run. This current source is in series with a RF device, and a source resistor. Notice how the voltage is not correlated with the current, thus providing a constant drain voltage.

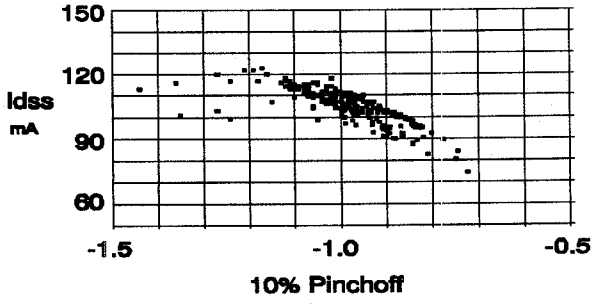

Figure 5. A 300u PHEMT Idss vs. Pinch-off.

RESULTS

Special considerations were incorporated to make this amplifier stable with high gain and low noise figure. For low noise amplification, the LNA uses a common source first stage and a source follower second stage with resistive feedback. This unique configuration provided the unlikely combination of a optimum noise figure below 1.3 dB with associated maximum available gain of 16 dB (see Figure 7). Without external matching, the input and output Return Loss are typically -6 dB (see Figure 8). A narrow band input match below -17 dB Return Loss is achieved through the addition of input series inductance (see Figure 10). This is at the expense of optimum noise figure and gain. A typical noise figure of 1.7 dB and gain of 15 dB is acheived with an external match. The output power exceeds +3 dBm (see Figure 9) giving the MMIC a high dynamic range.

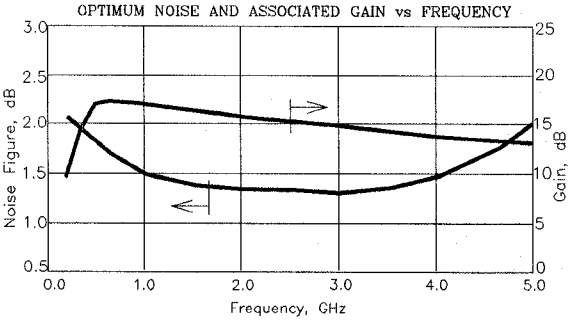

Figure 7. Optimum noise figure and associated gain as measured on wafer.

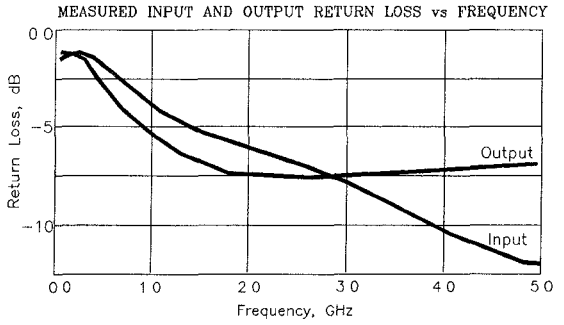

Figure 8. Typical return loss as measured in a carrier.

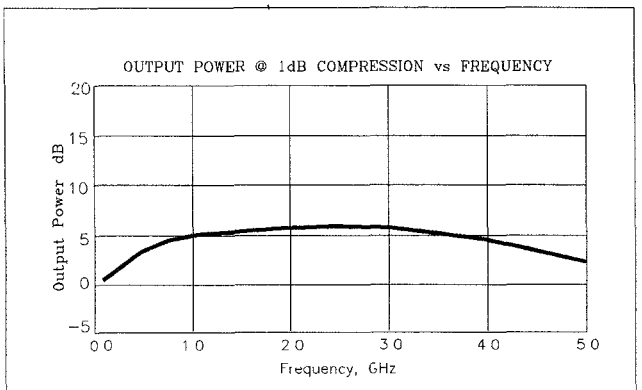

Figure 9. Output power at 1dB compression as measured on a carrier.

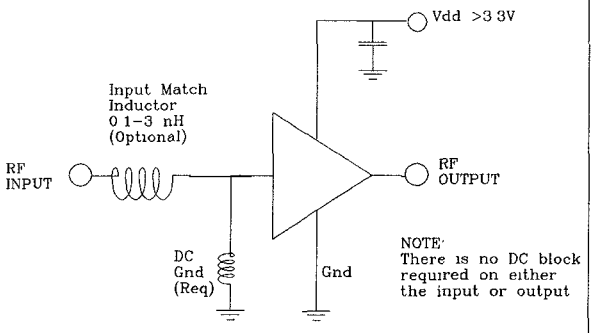

Figure 10. Typical biasing and input matching configuration.

APPLICATIONS

The DC requirements for this amplifier are designed with battery users in mind. The MMIC requires only a single 3.3 Volt supply and draws an average of 15 mA. Best power and gain results are achieved with a 4.5V supply. The RF input and output are at a nominal 0V, thus no RF blocking capacitors are needed. The combination of these characteristics make the chip ideal for high volume, surface mount applications.

Figure 10 demonstrates a typical bias and matching circuit used in the application of the LNA. The chip requires no bias choke, although a simple DC filter bypass is recommended to isolate DC power. The input series inductance can be varied from 0.1 to 5 nH to achieve optimal input match. The MMIC is unconditionally stable over the entire frequency of operation.

CONCLUSIONS

A monolithic low noise amplifier using PHEMT technology has been demonstrated over the 500MHz to 3 GHz band. The chip is unique in utilization of a source follower second stage, resistive feedback, and on chipcurrent sources. The monolithic chip has over 15 dB of gain with an associated noise figure below 1.7. The chip has also demonstrated the ability to operate off a single 3.3V supply, draws less than 15 mA of current, and requires no bias choke. The die is small (0.375 mm sq) and designed to fit in a variety of plastic packages. These are state of the art results for a low noise, low dc power, low cost MMIC amplifiers for GPS and spread spectrum applications.

ACKNOWLEDGMENT

The authors wish to thank John Coward and Hue Tran for their technical assistance and Ding Day, John Wei, and K.Y. Ramanujam for fabrication. They also wish to thank Craig P. Snapp for his support.

REFERENCES

[1] P.M. Smith, P.C. Chao, K.H. Duh, L.F. Lester, B.R. Lee, and J. M. Ballingall, "Advances in HEMT Technology and Applications", 1987 IEEE MTT-S International Symposium Digest, p 749.

[2] N. Camilleri, P. Chye, A. Lee, P. Gregory, "Monolithic 9 to 70 GHz Distributed Amplifier", 1990 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest, p 27-30.

[3] Copyright 1991, Cascade Microtech Inc., Noise Parameter Test System for IBM PC/AT, 14255 S. W. Brigadoon Court, Beaverton, Oregon 97005.

[4] M. Frank, "The Current Source as a Microwave Biasing Element", US Patent # 4,912,430.

[5] M. Frank, "The 2 to 6 GHz, 10 Block GaAs MMIC Amplifier", Microwave Journal, August 1990, pp. 83-92.

[6] C. Yuen, M. Raiziat, S. Bandy, G. Zdasiuk, "Application of HEMT Devices to MMICs," Microwave Journal, August 1988, vol. 31, No. 8, pp 87-104.